Exhibit B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	JERRY W. YANCEY ET AL.
Filed:	NOVEMBER 16, 2006
For:	RECONFIGURABLE COMMUNICATIONS INFRASTRUCTURE FOR ASIC NETWORKS
Serial No.:	11/600,934
Group Art Unit:	2112
Examiner:	BAKER, STEPHEN M.
Atty Dkt:	LCOM:057

Pursuant to 37 C.F.R. 1.8, I certify that this correspondence is being deposited with the U.S. Postal Service in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313 on the date below:

10/25/10 Matt Pons

Date Name

Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

I. AMENDMENT; and

II. RESPONSE TO OFFICE ACTION DATED JUNE 23, 2010

Sir:

This paper is submitted in response to the Office Action dated June 23, 2010.

A Request For Extension Of Time To Respond To Office Action Dated June 23, 2010 is being filed concurrently herewith.

Reconsideration of the application is respectfully requested.

I. AMENDMENT

In the Specification:

Please amend paragraph 0099 as follows:

[0099] Reconfigurable communications infrastructure 1300 of Figures 13-15 may be configured in one exemplary embodiment with a PRISM routing scheme that provides a duplex data communication link between each FPGA of a given signal processing circuit (*e.g.,* circuit card) and high bandwidth interface 1510 (*e.g.,* PMC interface site 124 of Figure 1) with high bandwidth interconnection medium 1350. In such a configuration, a data packet may be routed from a given source of a source computing device (*e.g.,* FPGA 1320) of a first reconfigurable signal processing circuit to a given destination of a destination computing device (*e.g.,* a different FPGA 1320) of a second reconfigurable signal processing circuit using, for example, PRISM router and data packet configurations illustrated and described herein in relation to Figures 5, 6 and 7. However, it will be understood that any other data packet configuration and routing scheme suitable for allowing a sender or source to determine the packet's destination within a reconfigurable communications infrastructure 1300 may be employed (*e.g.,* TCP/IP, Fibrechannel, XAUI, Ethernet, Infiniband, Rapid I/O, *etc.*). Further information on exemplary methodology and systems that may be employed for relaying data packets in the disclosed systems and methods may be found in United States Patent Application Serial No. [[_____]] 11/600,935, entitled "METHODS AND SYSTEMS FOR RELAYING DATA PACKETS" by Yancey, et al. (Atty. Docket LCOM-056) filed on the same date as the present application and which is incorporated herein by reference.

In the Claims:

Please amend claims 1-24, 27, 29-31 and 33-34 as follows. This listing of claims will replace all prior versions, and listings, of claims for the present application:

1. (Currently Amended) A method, comprising:

providing two or more separate signal processing circuits, each one of said two or more signal processing circuits including multiple ASIC devices that each includes ~~ASIC devices, each one of said two or more ASIC devices comprising~~ a respective packet router;

providing a high bandwidth interconnection medium coupled between said signal processing circuits ~~packet routers of each of said two or more ASIC devices~~ to form a reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being selectively segregatable from each other, and the respective ASIC devices of each one of said two or more signal processing circuits being directly coupled to said high bandwidth interconnection medium by a respective common interface provided for the ASIC devices of each of said two or more signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices; and

selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of each of the respective ASIC devices of each one of said signal processing circuits ~~two or more ASIC devices~~ across ~~said~~ a first common interface to the high bandwidth interconnection medium and to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective

ASIC devices of said other one of said signal processing circuits without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium.

2. (Currently Amended) The method of claim 1, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

3. (Currently Amended) The method of claim 9 [[2]], wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router;~~

~~providing said high bandwidth interconnection medium coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and~~

~~communicating data across said high bandwidth interconnection medium between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

4. (Currently Amended) The method of claim 2 [[3]], wherein ~~at least one of~~ each of said signal processing circuits is a reconfigurable signal processing circuit that ~~further~~ comprises two or

more FPGA devices that each ~~comprise~~ includes a packet router, said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ being coupled to each respective packet router of each of the other of said two or more FPGA devices of said ~~at least one~~ same given one of said signal processing circuits ~~circuit~~; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ to communicate data packets within said given signal processing circuit by routing data packets to and from ~~with~~ each other of said two or more FPGA devices of the same given one of said ~~at least one~~ signal processing circuits ~~circuit~~ without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

5. (Currently Amended) The method of claim 4, wherein said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ is coupled to each respective packet router of each of the other of said two or more FPGA devices of same said ~~at least one~~ same given one of said signal processing circuits ~~circuit~~ by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said same given one of said signal processing circuits ~~circuit~~; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices of said each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ to transmit and receive data packets across each of said separate respective duplex data communication links existing between said given one of said two or more FPGA devices and each other of said two or more FPGA devices of the same given one of said ~~at least one~~ signal processing circuits ~~circuit~~ without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

6. (Currently Amended) The method of claim 2, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises user-defined circuitry coupled

to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said user-defined circuitry of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

7. (Currently Amended) The method of claim 2, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises at least one embedded processor coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said method further comprises transmitting and receiving data packets between said at least one embedded processor of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

8. (Currently Amended) The method of claim 2, further comprising providing a vehicle-based reconfigurable communications infrastructure comprising a vehicle with each of said two or more ~~FPGA devices~~ signal processing circuits and said high bandwidth interconnection medium being positioned on or within said vehicle; and communicating data between said two or more signal processing circuits through said packet routers of each of said ~~two or more~~ FPGA devices of said two or more signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium on or within said vehicle.

9. (Currently Amended) The method of claim 2, further comprising providing said two or more signal processing circuits ~~FPGA devices~~ in positions physically segregated from each other; and communicating data between said packet router ~~routers~~ of a respective one said FPGA devices of each of said two or more physically-segregated signal processing circuits ~~FPGA devices~~ across

said first and second common interfaces and through said high bandwidth interconnection medium to the packet router of a respective FPGA device of an other one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

10. (Currently Amended) The method of claim 2, wherein said high bandwidth interconnection medium comprises an optical transmission medium; and wherein said method further comprises selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of a respective FPGA device of each one of said two or more signal processing circuits ~~FPGA devices~~ across said first and second common interfaces and through said optical transmission medium to a respective FPGA device of an other different one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

11. (Currently Amended) The method of claim 2, further comprising selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router ~~routers~~ of a respective FPGA device of each one of said two or more signal processing circuits ~~FPGA devices~~ at a data transmission rate of greater than or equal to about 1 Gbps to a respective FPGA device of an other different one of said signal processing circuits without routing said data through any other intervening processing device between each respective FPGA device and the high bandwidth interconnection medium.

12. (Currently Amended) The method of claim 2, further comprising configuring each of said at least two separate signal processing circuits ~~FPGA devices~~ to perform different computing tasks in parallel.

13. (Currently Amended) The method of claim 2, further comprising:

providing said two or more separate signal processing circuits ~~FPGA devices~~ as a first signal processing circuit ~~first~~ and a second signal processing circuit ~~FPGA devices~~;

configuring said first and second signal processing circuits ~~FPGA devices~~ to perform a first computing task together as a first computing cluster;

providing at least two additional separate signal processing circuits ~~FPGA devices~~ as a third signal processing circuit including multiple FPGA devices and a fourth signal processing circuit including multiple FPGA devices, the first, second, third and fourth signal processing circuits being selectively segregatable from each other and each one of said respective FPGA devices of said third and fourth signal processing circuits ~~FPGA devices comprising a packet router~~ being directly coupled to said high bandwidth interconnection medium by a respective common interface provided for the FPGA devices of each of said third and fourth signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and the FPGA devices of said respective third and fourth signal processing circuits;

dynamically configuring said third and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a second computing task together as a second computing cluster, said second computing task being different than said first computing task; and

simultaneously performing said first computing task with said first computing cluster and said second computing task with said second computing cluster.

14. (Currently Amended) The method of claim 13, further comprising:

dynamically reconfiguring said first and third separate signal processing circuits ~~FPGA devices~~ in real time to perform a third computing task together as a third computing cluster;

dynamically configuring said second and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a fourth computing task together as a fourth computing cluster, said fourth computing task being different than said third computing task; and

simultaneously performing said third computing task with said third computing cluster and said fourth computing task with said fourth computing cluster.

15. (Currently Amended) The method of claim 13, further comprising:

dynamically reconfiguring said first, second, third and fourth separate signal processing circuits ~~FPGA devices~~ in real time to perform a third computing task together as a third computing cluster; and

performing said third computing task with said third computing cluster.

16. (Currently Amended) A reconfigurable communications infrastructure, comprising:

two or more separate signal processing circuits, each one of said two or more signal processing circuits including at multiple ASIC devices that each includes ~~ASIC devices, each one of said two or more ASIC devices comprising~~ a respective packet router; and

a high bandwidth interconnection medium coupled between said signal processing circuits ~~packet routers of each of said two or more ASIC devices~~ to form said reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being selectively segregatable from each other, and the respective ASIC devices of each one of said two or more signal processing circuits being directly coupled to said high bandwidth interconnection medium by a common interface provided for the ASIC devices of each of said two or more signal processing circuits with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices; and

wherein the reconfigurable communications infrastructure is configured to selectively communicate data between said two or more signal processing circuits by selectively routing data through the packet router of each of the respective ASIC devices of each one of said signal processing circuits across a first common interface said high bandwidth interconnection medium to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective ASIC devices of said other one of said signal processing circuits without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium ~~provide data communication between said packet routers of each of said two or more ASIC devices~~.

17. (Currently Amended) The reconfigurable communications infrastructure of claim 16, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

18. (Currently Amended) The reconfigurable communications infrastructure of claim 24 ~~17~~, wherein said two or more signal processing circuits are physically segregated from each other by

at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and~~

~~wherein said high bandwidth interconnection medium is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

19. (Currently Amended) The reconfigurable communications infrastructure of claim 17 ~~18~~, wherein ~~at least one~~ each of said signal processing circuits is a reconfigurable signal processing circuit that ~~further~~ comprises two or more FPGA devices that each ~~comprise~~ includes a packet router, said packet router of each one of said two or more FPGA devices of each given on of said ~~at least one~~ signal processing ~~circuit~~ circuits being coupled to each respective packet router of each of the other of said two or more FPGA devices of said same given one of said ~~at least one~~ signal processing circuits ~~circuit~~; and wherein said packet router of each given one of said two or more FPGA devices of said signal processing circuits is configured to communicate data packets within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices of the same given one of said signal processing circuits without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

20. (Currently Amended) The reconfigurable communications infrastructure of claim 19, wherein said packet router of each one of said two or more FPGA devices of each given one of said ~~at least one~~ signal processing circuits ~~circuit~~ is coupled to each respective packet router of each of the other of said two or more FPGA devices of same said ~~at least one~~ same given one of

said signal processing ~~circuit~~ circuits by a separate respective duplex data communication link so as to form a direct serial interconnection between each two of said two or more FPGA devices of said same given one of said signal processing circuits ~~circuit~~; and wherein said packet router of each given one of said two or more FPGA devices of each given one of said signal processing circuits is configured to communicate data packets within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices of the same given one of said signal processing circuits without routing said data packets outside said given signal processing circuit across said first or second common interfaces to said high bandwidth interconnection medium.

21. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises user-defined circuitry coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said respective packet router of each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits is configured to transmit and receive data packets between said user-defined circuitry of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across said first and second common interfaces and through said high bandwidth interconnection medium.

22. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits comprises at least one embedded processor coupled to said respective packet router of said given one of said ~~two or more~~ FPGA devices; and wherein said respective packet router of each given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits is configured to transmit and receive data packets between said at least one embedded processor of said given one of said ~~two or more~~ FPGA devices of one of said signal processing circuits and an other one of said FPGA devices of an other different one of said signal processing circuits across

said first and second common interfaces and through said high bandwidth interconnection medium.

23. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein said reconfigurable communications infrastructure is a vehicle-based reconfigurable communications infrastructure comprising a vehicle; and wherein each of said two or more ~~FPGA devices~~ signal processing circuits, first and second common interfaces, and said high bandwidth interconnection medium is positioned on or within said vehicle.

24. (Currently Amended) The reconfigurable communications infrastructure of claim 17, wherein said two or more ~~FPGA devices~~ signal processing circuits are physically segregated from each other.

25. (Original) The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an optical transmission medium.

26. (Original) The reconfigurable communications infrastructure of claim 17, wherein said high bandwidth interconnection medium comprises an interconnection medium having a data transmission capability of greater than or equal to about 1 Gbps.

27. (Currently Amended) A communications infrastructure, comprising two or more ~~ASIC devices~~ separate signal processing circuits, each one of said two or more ~~ASIC devices~~ signal processing circuits including multiple ASIC devices that each itself includes ~~comprising~~ a packet router, said packet router of each one of said ~~two or more~~ ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a ~~each~~ respective

packet router of each of the ASIC devices of each other of said two or more ~~ASIC devices~~ signal processing circuits ~~by an interconnection comprising a high speed serial optical link~~ with no other processing device intervening between the high speed optical link and said ASIC devices of each of said two or more signal processing circuits.

28. (Original) The communications infrastructure of claim 27, wherein said interconnection further comprises a high bandwidth interconnection medium.

29. (Currently Amended) The communications infrastructure of claim 28, wherein each of said ~~two or more~~ the ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

30. (Currently Amended) The communications infrastructure of claim 27 ~~29~~, wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other ~~further comprising:~~

~~two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router; and~~

~~wherein said interconnection is coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

31. (Currently Amended) A method, comprising:

providing two or more ~~ASIC devices~~ separate signal processing circuits, each one of said two or more ~~ASIC devices~~ signal processing circuits including multiple ASIC devices that each itself includes ~~comprising~~ a packet router, said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits being coupled through respective first and second common interfaces and an intervening high speed serial optical link to a respective packet router of each of the other ASIC devices of each other of said two or more signal processing circuits ~~coupled together~~ ~~by an interconnection comprising a high speed serial optical link~~ with no other processing device intervening between the high speed serial optical link and said ASIC devices of each of said two or more signal processing circuits, and

selectively transferring at least one data packet from each said packet router of each one of said ASIC devices of each given one of said respective two or more signal processing circuits ~~ASIC devices~~ to each respective packet router of said at ASIC devices of each of the other of said two or more signal processing circuits ~~ASIC devices~~ through said first and second common interfaces and said intervening ~~by said~~ high speed serial optical link without routing said data through any other intervening processing device between each respective ASIC device and the high speed serial optical link.

32. (Original) The method of claim 31, wherein said interconnection further comprises a high bandwidth interconnection medium.

33. (Currently Amended) The method of claim 32, wherein each of said ~~two or more~~ ASIC devices of said two or more signal processing circuits is an FPGA device ~~comprises FPGA devices~~.

34. (Currently Amended) The method of claim 31 ~~33~~, ~~further comprising:~~ wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other

~~providing said two or more FPGA devices by providing two or more signal processing circuits, each one of said two or more signal processing circuits comprising at least one FPGA device that comprises a packet router;~~

~~providing said interconnection coupled between said two or more signal processing circuits to provide data communication between said packet routers of said FPGA devices of each of said two or more signal processing circuits; and~~

~~communicating data across said interconnection between said packet routers of said FPGA devices of each of said two or more signal processing circuits~~.

II. RESPONSE TO OFFICE ACTION

Claims 1-24, 27, 29-31 and 33-34 have been amended to even more particularly point out and claim the subject matter of the claims. Claims 1-34 are pending.

A. The Objections to the Specification

Paragraph 0099 has been amended to address the objection regarding copending application data.

Contrary to the assertion in the Office Action, the terms "ASIC" and "FPGA" are used in an appropriate manner in the Specification, for example, in paragraph 0010 of the Specification which states that "[e]xamples of ASIC devices that may be interconnected using the disclosed systems and methods include, but are not limited to, Field Programmable Gate Arrays ("FPGAs") or other field programmable devices ("FPDs") or programmable logic devices ("PLDs")."

As evidence that FPGAs, FPDs and PLDs are each types of ASIC devices, Applicants submit herewith the attached definition of the term "ASIC" as Exhibit A. As clearly shown on page 2 of Exhibit A, the term "ASIC" embraces field programmable devices such as FPGAs. Each of the paragraphs of the Specification identified on page 2 of the Office Action uses these terms in a manner consistent with this definition. Thus, the usage of these terms in the Specification is entirely proper, and the objection to the Specification should be withdrawn.

Favorable reconsideration is requested.

B. The 35 USC Section 112 Rejections

Contrary to the rejections of the claims made on pages 2-3 of the Office Action, the usage of "ASIC devices" in these claims is clear (*see* Exhibit A and the discussion above regarding the objections to the Specification). Moreover, Applicants note that "it is a fundamental principal

that Applicants may be their own lexicographers, and that they "can define in the claims what they regard as their invention essentially in whatever terms they choose" and "a claim may not be rejected solely because of the type of language used to define the subject matter for which patent protection is sought" (*see* MPEP 2173.01). However, in the present case, the language of Applicants' claims is already consistent with the definition of the term "ASIC", and is thus completely acceptable for this reason alone.

Although claim 3 has been amended for other purposes, Applicants also disagree with the rejection of the previous wording of claim 3 on page 3 of the Office Action because this claim was entirely clear as previously worded. To illustrate, Applicants refer to the exemplary embodiment of Figure 13 and paragraph 0089 of the Specification which describes how in this embodiment "reconfigurable communications infrastructure 1300 includes at least four *separate signal processing circuits* (*e.g.,* four separate circuit cards) 1310, 1312, 1314 and 1316 **[and]** signal processing circuit 1310 includes a single ASIC device in the form of *a FPGA 1320*, signal processing circuit 1312 includes a single processor device (*e.g.*, CPU, microprocessor), signal processing circuit 1314 includes an array of four ASIC devices in the form of *four FPGAs 1320*, and signal processing circuit 1316 includes an array of two ASIC devices in the form of *two FPGAs 1320*" (emphasis added). Accordingly, referring to the non-limiting example of Figure 13, the previous wording of claim 3 recited (in part) "providing said two or more FPGA devices **[*e.g.*, 1320]** by providing two or more signal processing circuits **[*e.g.*, 1310, 1314 or 1316]** each one of said two or more signal processing circuits **[*e.g.*, 1310, 1314 or 1316]** comprising at least one FPGA device **[*e.g.*, 1320]**." In other words, two or more FPGA devices are provided by supplying two or more signal processing circuits (*e.g.,* as two separate circuit cards) that each itself includes at least one FPGA device. The previous wording of claim 3 was thus not only clear, but also consistent with the description and illustrated embodiments of the Specification.

Next, the interpretation of claim 4 made on pages 3-4 of the Office Action is incorrect, and the present language of this claim is clear and definite for the following reasons. To illustrate, Applicants refer to the exemplary embodiment of Figure 15 and paragraph 0095 of the Specification that describes how in this embodiment "*reconfigurable signal processing circuit* 1314 includes four FPGA devices that may be configured to communicate with each other in a manner as described for FPGA devices 102, 104, 106 and 108 of Figures 1-12 herein, *i.e.,* with

duplex serial data communication links 1520 provided between each given two of FPGA devices 102, 104, 106 and 108 (*e.g.,* via high speed serial I/O connections in the form of MGTs), and with each FPGA being provided with *a packet router* interface switch matrix ("PRISM") to route packets between each of the individual FPGA devices via respective *duplex serial data communication links 1520* as shown" (emphasis added). Accordingly, referring to the non-limiting example of Figure 15, amended dependent claim 4 recites (in part) "said packet router of each one of said two or more FPGA devices **[*e.g.,* 1320]** of each given one of said signal processing circuits **[*e.g.,* 1314]** being coupled **[*e.g.,* via data communication links 1520]** to each respective packet router of each of the other of said two or more FPGA devices **[*e.g.,* 1320]** of said same given one of said signal processing circuits **[*e.g.,* 1314]**; and wherein said method further comprises using said packet router of each given one of said two or more FPGA devices **[*e.g.,* 1320]** of each given one of said signal processing circuits **[*e.g.,* 1320]** to communicate data packets **[*e.g.,* across data communication links 1520]** within said given signal processing circuit by routing data packets to and from each other of said two or more FPGA devices **[*e.g.,* 1320]** of the same given one of said signal processing circuits **[*e.g.,* 1314]**". In other words, the packet router of each of the FPGA devices of a given signal processing circuit is coupled to the packet router of each of the other FPGA devices of the same given signal processing circuit, for example, by the communication links 1520 of Figure 15. Claim 4 is thus not only clear, but also consistent with the description and illustrated embodiments of the Specification. Similar reasoning applies the 35 USC Section 112 rejection of claims 5, 19 and 20.

With regard to claim 15, this claim has been amended to recite (in part) "performing said third computing task with said third computing cluster.

As shown above, all of the pending claims are clear and definite. Favorable reconsideration is requested.

C. The 35 USC Section 103 Rejections

Amended independent claim 1 recites:

> A method, comprising: providing two or more separate signal processing circuits, each one of said two or more signal processing circuits including multiple ASIC devices that each includes a respective packet router; providing a high bandwidth interconnection medium coupled between said signal processing circuits to form a reconfigurable communications infrastructure of said two or more signal processing circuits, the two or more signal processing circuits being *selectively segregatable* from each other, and *the respective ASIC devices* of each one of said two or more signal processing circuits *being directly coupled to* said high bandwidth interconnection medium by *a respective common interface* provided for the ASIC devices of each of said two or more signal processing circuits *with no other processing device intervening between the high bandwidth interconnection medium and said respective ASIC devices*; and selectively communicating data between said two or more signal processing circuits by selectively routing data through the packet router of each of the respective ASIC devices of each one of said signal processing circuits across a first common interface to the high bandwidth interconnection medium and to an other one of said signal processing circuits through a second common interface to the packet router of each of the respective ASIC devices of said other one of said signal processing circuits *without routing said data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium.*

The Office Action cites Col. 5, lines 61-64 of Mukherjee to reject original claim 1. However Mukherjee's "system **10**" is implemented using "SPM methodology **14** [which] is the *software* methodology and tool that implements application designs onto the hybrid network **12**" that is further illustrated in Figure 2 (*see* Col. 5, line 66 to Col. 6, line 1; *see also* Figure 1)(emphasis added). In particular, the Office Action points to the "example network (12) topologies mentioned by Mukherjee" and states that "communications between Mukherjee's network nodes can be said to provide a 'high bandwidth interconnection medium' forming a 'reconfigurable communications infrastructure" (*see* pages 4-5 of the Office Action).

However, unlike amended claim 1, Mukherjee teaches or suggest nothing regarding two or more separate signal processing circuits that each includes multiple ASIC devices that are each *directly coupled to* a high bandwidth interconnection medium by a respective common interface *with no other processing device intervening between the high bandwidth interconnection medium and the respective ASIC devices.* Rather each of the nodes of Mukherjee's network 12 requires an intervening "host machine 22" which connects the node to the network 12 (*see* Figure 2) and which further requires that "one of the nodes 22 functions as a master server 20 in that it provides the interconnection point between the network 12 and the SPM tool 14. It is the master server 20 on which the SPM tool 14 is installed" (*see* Col. 6, lines 24-27).

Thus Mukherjee actually *teaches away* from the recitation of amended claim 1, which relates to a method in which *the respective ASIC devices* of each one of the two or more signal processing circuits *are directly coupled to* the high bandwidth interconnection medium *with no other processing device intervening between the high bandwidth interconnection medium and the respective ASIC devices,* as well as the step of selectively communicating data *between the two or more signal processing circuits* by selectively routing data through the packet router of each of the respective ASIC devices of each one of the signal processing circuits to the packet router of each of the respective ASIC devices of the other one of the signal processing circuits *without routing the data through any other intervening processing device between each respective ASIC device and the high bandwidth interconnection medium* (*see* MPEP 2141.02).

For at least the above reasons, amended independent claim 1, and the claims dependent therefrom are thus not obvious over the cited reference. Similar reasoning applies to amended independent claims 16, 27 and 31, as well as the claims dependent from these amended independent claims.

The Office Action admits that a number of the claimed limitations are missing from Mukherjee, but nonetheless relies on "Official Notice" to satisfy these deficiencies of the reference and reject numerous claims. In particular the Office Action cites to "Official Notice" on four separate occasions (*see* the Office Action at pages 5, 6 and 7). Applicants note that MPEP 2144.03 states that "[o]fficial notice unsupported by documentary evidence should only be taken by the examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of **instant and unquestionable demonstration** as being well-known [and] the notice of facts beyond the record which may be taken by the examiner must be "capable of such instant and unquestionable demonstration as to defy dispute" (emphasis added). Thus, "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known" (*see Id.*) (emphasis added). Importantly, "[t]he Board cannot simply reach conclusions based on its own understanding or experience-or on its assessment of what would be basic knowledge or common sense" (*see Id.*) **Rather, "[i]f the examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting forth**

specific factual statements and explanation to support the finding" (*see Id.*). Thus, if rejections based on "Official Notice" are to be maintained in the next Office Action, the Examiner is respectfully requested to either provide one or more references in support of the rejections, or an affidavit averring facts within the personal knowledge of the Examiner.

Favorable reconsideration is requested.

D. The Dependent Claims

The dependent claims include additional limitations that render these claims even further nonobvious over Mukherjee. For example, amended dependent claim 3 recites "wherein said two or more signal processing circuits are physically segregated from each other by at least one of being positioned *in different rooms of a given building or facility from each other, or being positioned in different compartments of a given mobile vehicle from each other*" (emphasis added). Similar reasoning applies to amended dependent claims 18, 30 and 34.

As another example, amended dependent claim 13 recites, in part, "configuring said first and second *signal processing circuits* to perform a first computing task together as *a first computing cluster*", "providing at least two additional separate signal processing circuits as a third signal processing circuit including multiple FPGA devices and a fourth signal processing circuit including multiple FPGA devices, *the first, second, third and fourth signal processing circuits being selectively segregatable from each other*", and "dynamically configuring said third and fourth separate *signal processing circuits* in real time to perform a second computing task together as *a second computing cluster*, said second computing task being different than said first computing task; and *simultaneously performing* said first computing task with said first computing cluster and said second computing task with said second computing cluster" (emphasis added). Similar reasoning applies to amended dependent claims 14-15 which depend amended dependent claim 13, and which include additional "reconfiguring" limitations.

E. Conclusion

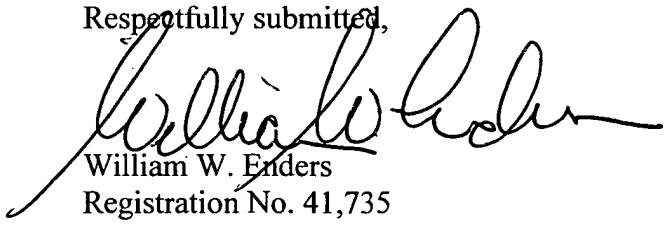
The pending claims have been shown above to be allowable over the cited references. Applicants therefore respectfully submit that claims are in condition for allowance. Reconsideration of the application and claims is courteously solicited.

Please find attached a check in the amount of $130.00 for the Request For Extension Of Time. No additional fees are believed to be due with respect to the enclosed materials. However, should any fees under 37 CFR 1.16-1.21 be required for any reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/LCOM:057.

In accordance with 37 CFR 1.136(a)(3), the Commissioner is authorized to treat any concurrent or future reply that requires a petition for an extension of time under 37 CFR 1.126(a) to be timely, as incorporating a petition for extension of time for the appropriate length of time, and the Commissioner is authorized to deduct any requisite extension of time fees under 37 CFR 1.16 to 1.21 from Deposit Account No. 10-1205/ LCOM:057.

The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,



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